In the claims:

For the Examiner's convenience, all pending claims are presented below.

1. (Previously Presented) An apparatus, comprising:

an integrated circuit including:

a first processor with a first dedicated cache;

a second processor with a second dedicated cache; and

control logic coupled to the first and second dedicated caches to receive a first cache line from the first dedicated cache and to transfer the first cache line to the second dedicated cache.

2. (Previously Presented) The apparatus of claim 1, wherein:

the control logic is to transfer the first cache line if the first cache line is a cache line in the first dedicated cache and not in the second dedicated cache.

3. (Previously Presented) The apparatus of claim 1, wherein:

the control logic is to transfer the first cache line if the first cache line is a modified version of a particular cache line and the second dedicated cache contains an unmodified version of the particular cache line.

4. (Original) The apparatus of claim 1, further comprising:

a coherency unit to perform snoop operations on the first and second dedicated caches.

5. (Previously Presented) The apparatus of claim 1, wherein:

the control logic is further to transfer a second cache line from the second dedicated cache to the first dedicated cache.

6. (Previously Presented) The apparatus of claim 1, wherein the integrated circuit further includes:

a shared cache coupled to the control logic and to the second dedicated cache to provide the first cache line to the second dedicated cache;

wherein the control logic includes a write buffer to receive the first cache line from the first dedicated cache and to provide the first cache line to the shared cache.

7. (Previously Presented) The apparatus of claim 1, wherein the integrated circuit further includes:

a shared cache coupled to the control logic, to the first dedicated cache, and to the second dedicated cache;

wherein the control logic is further to transfer a second cache line from the second dedicated cache to the first dedicated cache;

wherein the control logic includes a first write buffer to receive the first cache line from the first dedicated cache and to provide the first cache line to the shared cache, and further includes a second write buffer to receive the second cache line from the second dedicated cache and provide the second cache line to the shared cache;

wherein the shared cache is to provide the first cache line to the second dedicated cache and to provide the second cache line to the first dedicated cache.

8. (Previously Presented) The apparatus of claim 1, wherein:

the control logic includes a fill buffer coupled to first and second dedicated caches to receive the first cache line from the first dedicated cache and to provide the first cache line to the second dedicated cache.

9. (Previously Presented) The apparatus of claim 1, wherein:

the control logic includes a first fill buffer coupled to the first and second dedicated caches to receive the first cache line from the first dedicated cache and to provide the first cache line to the second dedicated cache; and

the control logic includes a second fill buffer coupled to the first and second dedicated caches to receive a second cache line from the second dedicated cache and to provide the second cache line to the first dedicated cache

10. (Previously Presented) The apparatus of claim 1, wherein the control logic includes:

a multiplexer coupled to the first and second caches to receive the first cache line from the first dedicated cache and to provide the first cache line to the second dedicated cache.

11. (Previously Presented) The apparatus of claim 1, wherein the control logic includes:

a first multiplexer coupled to the first and second caches to receive the first cache line from the first dedicated cache and to provide the first cache line to the second dedicated cache; and

a second multiplexer coupled to the first and second caches to receive a second cache line from the second dedicated cache and to provide the second cache line to the first dedicated cache.

12. (Previously Presented) A method, comprising:

transferring a first cache line from a first dedicated cache of a chip multi-processor to control logic in the chip multi-processor; and

subsequently transferring the first cache line from the control logic to a second dedicated cache of the chip multi-processor.

13. (Previously Presented) The method of claim 12, further comprising:

transferring a second cache line from the second dedicated cache to the control logic, entirely within the chip multi-processor; and

subsequently transferring the second cache line from the control logic to the first dedicated cache, entirely within the chip multi-processor.

14. (Previously Presented) The method of claim 12, wherein:

the transferring the first cache line from the first dedicated cache includes transferring the first cache line from the first dedicated cache to a write buffer;

the transferring the first cache line from the control logic includes transferring the first cache line from the write buffer to a shared cache.

15. (Previously Presented) The method of claim 14, wherein:

the transferring the first cache line from the control logic further includes transferring the first cache line from the shared cache to the second dedicated cache.

16. (Previously Presented) The method of claim 12, wherein:

the transferring the first cache line from the first dedicated cache includes transferring the first cache line from the first dedicated cache to a fill buffer;

the transferring the first cache line from the control logic includes transferring the first cache line from the fill buffer to the second dedicated cache.

17. (Previously Presented) The method of claim 12, wherein:

the transferring the first cache line from the first dedicated cache includes transferring the first cache line from the first dedicated cache to a multiplexer; and

the transferring the first cache line from the control logic includes transferring the first cache line from the multiplexer to the second dedicated cache.

18. (Previously Presented) A system, comprising:

a main memory,

a chip multiprocessor coupled to the main memory and including:

a first processor with a first dedicated cache;

a second processor with a second dedicated cache; and

control logic coupled to the first and second dedicated caches to receive a first cache line from the first dedicated cache and to transfer the first cache line to the second dedicated cache.

19. (Previously Presented) The system of claim 18, wherein:

the control logic is further to a transfer second cache line from the second dedicated cache to the first dedicated cache entirely within the chip multiprocessor.

20. (Previously Presented) The system of claim 18, wherein the chip multiprocessor further includes:

a shared cache coupled to the control logic and to the second dedicated cache to provide the first cache line to the second dedicated cache;

wherein the control logic includes a write buffer to receive the first cache line from the first dedicated cache and to provide the first cache line to the shared cache.

21. (Previously Presented) The system of claim 18, wherein:

the control logic includes a fill buffer coupled to first and second dedicated caches to receive the first cache line from the first dedicated cache and to provide the first cache line to the second dedicated cache.

22. (Previously Presented) The system of claim 18, wherein the control logic includes:

a multiplexer coupled to the first and second dedicated caches to receive the first cache line from the first dedicated cache and to provide the first cache line to the second dedicated cache.

23. (Currently Amended) A tangible machine-readable medium that provides instructions, which when executed by a set of one or more processors, cause said set of processors to perform operations comprising:

transferring a cache line from a first dedicated cache in an integrated circuit to control logic in the integrated circuit, entirely within the integrated circuit; and

subsequently transferring the cache line from the control logic to a second dedicated cache of the integrated circuit.

24. (Previously Presented) The medium of claim 23, wherein:

the transferring the cache line from the first dedicated cache includes transferring the cache line from the first dedicated cache to a write buffer; and

the transferring the cache line from the control logic includes transferring the cache line from the write buffer to a shared cache and subsequently transferring the cache line from the shared cache to the second dedicated cache.

25. (Previously Presented) The medium of claim 23, wherein:

the transferring the cache line from the first dedicated cache includes transferring the cache line from the first dedicated cache to a fill buffer; and

the transferring the cache line from the control logic includes transferring the cache line from the fill buffer to the second dedicated cache.

26. (Previously Presented) The medium of claim 23, wherein:

the transferring the cache line from the first dedicated cache includes transferring the cache line from the first dedicated cache to a multiplexer; and

the transferring the cache line from the control logic includes transferring the cache line from the multiplexer to the second dedicated cache.